APPLICATION FOR

UNITED STATES LETTERS PATENT

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5   Blackwell, a citizen of United States, residing at 1733 Blake Bottom Road, Huntsville, Alabama 35806; Ayman Ghobrial, a citizen of Egypt, residing at 204 E. Royal Pines Drive, Huntsville, Alabama 35806; and Cynthia Lin, a citizen of United States, residing at 119 Caenstone Court, Madison, AL 35758, have invented a new and useful "Method and Apparatus for Duplex Transmission on

10   a Four Wire Communication System."

This application claims benefit of co-pending Provisional U.S. Patent Application Serial No. 60/156,039 filed September 24, 1999, entitled "Method and Apparatus for Duplex Transmission on a Four Wire Communication System" and Provisional U.S. Patent Application Serial No. 60/156,037 filed

15   September 24, 1999, entitled "Timing Device and Method Using A Timing Equalizer Filter for a Digital Communications System."

BACKGROUND OF THE INVENTION

This invention relates generally to dual-duplex, four-wire data

20   communications systems.

More particularly, this invention pertains to devices, systems and methods for effectively canceling differential transmission delays associated with data communications across a pair of communications loops.

A complex issue that arises in dual-duplex, four-wire data

5   communications systems is the separation (occurring at the sending end) and reconstruction (occurring at the receiving end) of data between the two wire pairs (loops). The incoming data to be transmitted must be split (usually evenly) between the two wire pairs at the input to the transmitters, and a single output data stream must be reconstructed from the two received data

10   streams at the output of the receivers. The reconstruction process is made more complicated in a four wire (A and B loop) system if there are differential time delays introduced by each of the loops, such that data symbols that are time aligned at the transmitters in the central office transceiver are not time aligned when they arrive at the receivers in the remote transceiver.

15   Two approaches for separation and reconstruction of transmitted data used in the prior art are: (1) transmission of data in blocks or frames on each wire pair; or (2) symbol-by-symbol interleaving of data between the pairs, where a "symbol" is a unique token conveying information. For example, in quadrature amplitude modulation (QAM), where the data signal is both

20   phase and amplitude modulated, each unique combination of amplitude and phase is a "symbol." In the first prior art approach, significant bandwidth,

referred to as framing overhead, may be required to allow correct de-framing of the data at the receiver. In the second approach, the framing overhead may be avoided by carefully measuring delays during training but this increases the complexity of the training sequence itself. In either of these

5   prior art approaches, interleaving or framing data buffers must be used in the transmitter, receiver, or in both. The use of such buffers introduces undesirable latency into the system.

What is needed, then, is a data communications device and method that can cancel the effects of differential transmission delay in a dual-duplex, four-

10 wire data communications system without increasing framing overhead, and without significantly adding to system latency.

SUMMARY OF THE INVENTION

The present invention provides a device and method for reliable

15 continuous communications of data in a dual-duplex, four-wire communications system where there may be a differential transmission delay between two communications loops connecting a central office and a remote location. In one embodiment, the invention forms an integral part of a system for full duplex transmission of a DS0 signal (64 Kbps), with an

20 overhead of 800 bits per second, providing a data rate per wire pair of 32.4 Kbps.

In one embodiment, the device comprises a dual channel transceiver having A and B channel transmitters functionally coupled to a data input through a data splitter. A and B channel receivers in the transceiver are coupled to a data output through a data combiner. Each of the A and B

5   channel transmitters are connected to corresponding A and B channel data scramblers and data mappers at their respective input stages and each of the A and B channel receivers are connected to respective A and B channel demappers and descramblers at their respective output stages.

In accordance with one novel feature of the invention, when the

10   transceiver is operated in a Training mode, the input to the A channel scrambler is functionally coupled to a source of training data so that a known sequence of training data can be transmitted. The input to the B channel mapper is switched from the output of the B channel scrambler to the output of the A channel scrambler so that the training data can be transmitted

15   concurrently across the A and B channels.

In one embodiment of the invention, each A and B channel receiver includes a both a decision feedback equalizer (DFE) and a linear equalizer (LEQ). During the Training mode, the data inputs to the A and B channel DFE's are switched to concurrently receive the same training data from a

20   training scrambler and mapper. Thus, in accordance with one novel feature of the invention, the A and B channel receivers are forced during the

Training mode to train together such that symbols that are transmitted together (time aligned in the transmitter) will always be time aligned after equalization in the receiver. In this way, the transmitter can simply accept sufficient bits of data to represent two symbols and allocate half of the bits to

5 each pair. In the receiver, the symbols are output concurrently and are reconstructed into a single data stream without any additional buffering.

The method of this invention does not require additional framing or delay to reconstruct the data stream from the A and B channels because the end-to-end delays associated with the A and B channels output bits are

10 adapted to be identical. The device and method can operate for extended periods across conventional telephone line pairs without the use of data buffers, and without requiring framing overhead or precise differential delay measurements.

15 **BRIEF DESCRIPTION OF THE DRAWINGS**

Fig. 1 is a block diagram showing first and second dual transceivers used in a dual-duplex, four-wire data communications system in accordance with the present invention.

Fig. 2 is a block diagram of a first embodiment of the dual transceivers

20 used in the system of Fig. 1, showing the A and B channel transmitters set to operate in a Training mode.

Fig. 3 is a block diagram of a first embodiment of the receiver section of one of the dual transceivers used in the system of Fig. 1, with the A and B channel receivers set to operate in a Data or Decision Directed mode.

Fig. 4 is a block diagram of a second embodiment of the transmitter

5   section of the dual transceivers used in system of Fig. 1, with the A and B channel transmitters set to operate in a Training mode.

Fig. 5 is a block diagram of a second embodiment of the receiver section of the dual transceivers used in the system of Fig. 1, with the A and B channel receivers set to operate in a Data or Decision Directed mode.

10   Fig. 6 is a flow chart showing the modes of operation of the dual transceivers in accordance with the present invention

Fig. 7 is a flow chart of an equalizer tap setting algorithm in accordance with the present invention.

Fig. 8 is a more detailed block diagram of one embodiment of a

15   transceiver that can be used to implement the method of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1 illustrates in block diagram form a dual-duplex, four wire data

20   communications system in accordance with the invention, having two dual transceivers 102, 104 coupled by two wire pairs 106, 108 for a total of 4 wires.

In one embodiment of the system, each wire pair 106, 108 is part of a conventional telephone line local loop (Loop A and Loop B on Figs. 2 through 5) wherein the first dual transceiver 102 is located at a telephone company central office (the "C-end") and the second dual transceiver 104 is located at a

5   remote site (the "R-end"). Thus, first dual transceiver 102 has a data input 110 connected to a source of data (not shown) that is to be transmitted, and a data output 122 where the data received from second dual transceiver 104 is provided. Similarly, second dual transceiver 104 has a data input 121 connected to an external data source (not shown) and a data output 111

10   where data received from first dual transceiver 102 is provided. In one embodiment, the system of Fig. 1 can be used for full duplex transmission of a standard DS0 signal having a nominal data rate of 64 Kbps with an overhead of 800 bps, with each wire pair (or loop) 106, 108 carrying 32.4 Kbps.

15   A block diagram of a first embodiment of the first dual transceiver 102 is shown in Fig. 2. In all material respects the dual transceivers 102, 104 are functionally identical. The data input 110 is connected to a data splitter 202 that splits the incoming data between A and B channel transmitters associated with data channels A and B. Each A and B channel and A and B

20   loop 106, 108 has its own transmitter but the two sections are functionally identical. Thus, the transmitter for each channel includes a data mapper

206, a shaping filter 208, modulator 210, and a D/A converter 212. The input to the A channel mapper 206A is connected to the output of A channel scrambler 204A, while the input to B channel mapper 206B is switched, as described below, between the outputs of A and B channel scramblers 204A

5   and 204B. The outputs of D/A converters 212A and 212B are connected to inputs on hybrid 214. The hybrid 214 includes interfaces to couple the transmitters and receivers to loop A (106) and loop B (108) and receiver outputs to receivers 220A and 220B. Thus, the hybrid 214 is a conventional device that directs the incoming and outgoing data to the proper transmitter

10   and receiver stage inside the transceiver. The respective outputs from A and B channel receivers 220A and 220B are connected to a data combiner 230. The output of data combiner 230 is connected to first transceiver output 122. The output of the data mapper 206 can also be communicated to an A channel echo canceller (not shown).

15   Each transmitter in dual transceivers 102, 104 operates in three modes: Pre-training, Training, and Data. In the Pre-training mode, the transceivers detect the presence or absence of load coils on each loop A and B and there is an exchange of pre-training system information between the dual transceivers 102, 104 using FSK modulation. This information can

20   include determining which is the A channel and which is the B channel and estimating line losses for purposes of setting the automatic gain control. In

the Training mode, uncoded 4-QAM signals are transferred between the transceivers 102, 104 over the two loops A and B as will be described in further detail below. During the Data mode, user data is transferred between a central office data node (C-end) and a data communications device

5   at the remote location (R-end).

Where the incoming user data is part of a 64 Kbps DS0 signal, the data is split on a symbol-by-symbol basis between channels A and B. During the Data mode, odd data bits are sent to the A channel transmitter through scrambler 204A and even data bits are send to the B channel transmitter

10   through scrambler 204B. In accordance with one novel aspect of the invention, during the Training mode (as shown in Fig. 2) the input of scrambler 204A is switched from the data splitter 202 to a source of training data, so that the training data for the A and B channels is identical, as each channel is driven by scrambler 204A.

15   In one embodiment, the system is operated in a coded 1024-QAM mode and the data splitter 202 splits a total of 18 bits for each symbol between the A and B channels. The data splitting is performed by numbering the 18 bits from 0 to 17, then causing the splitter 202 to send the even-numbered bits to channel A, and the odd-numbered bits to channel B. Other methods of data

20   splitting could also be applied, such as sending the first 9 bits of data to channel A and the second 9 bits to channel B.

Timing is important to proper functioning of the system. Therefore, the dual transceivers 102 and 104 are always clocked together in both transmitters and receivers. The C-end clock signal is derived from the data network or from an internal timing reference (not shown). The R-end clock

5   signal is derived from received timing from one of the wire pairs, such as on loop A (106).

A block diagram of a first embodiment of the first receiver section 220 is shown in Fig. 3. As is the case with the transmit sections, the relevant portions of the receive sections of the two channels are functionally identical.

10   The A channel receiver output from the hybrid 214 is connected to the input of an A/D converter 312A. The signal from A/D 312A is summed in summing stage 313A with the signal from A channel echo canceller (not shown). The resulting signal is then demodulated in demodulator 314A, and after passing through filter 316A, is processed in a linear equalizer (LEQ) 322A. The

15   primary function of the LEQ is to compensate for phase and amplitude distortion of the data signal caused by variable electrical characteristics of the loop, such as that introduced by the length of the loop and/or by the presence of load coils. The equalized data is then summed in summing stage 319A with the output from a decision feedback equalizer (DFE) 320A. The

20   summing stage 319A is coupled to a second summing stage 321A and to a decision module 322A that selects the received data symbol from the received

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data. The output of the decision module 322A is coupled to demapper 324A and descrambler 326A before the data is sent to combiner 230.

In the Data mode as shown on Fig. 3, the decision module 322A is coupled to DFE 320A and summing stage 321A. The summing stage 321A

5   sums output from decision module 322A with a signal from summing stage 319A. The output of the summing stage 321A is an error signal used to adapt the equalizer 318A and DFE 320A, as is known to those skilled in the art, using conventional equalizer algorithms.

In the Training mode, the data input to DFE 320A (and to DFE 320B

10   in receiver 220B) is switched to the output of training mapper 306, which is coupled to a training scrambler 304 to provide table directed training of the system. Thus, in accordance with yet another aspect of the invention, both equalizers 318A and 318B are trained using the same table directing training scrambler 304. Using this method, the received symbol timing between the A

15   and B channels is always concurrent, even if the two loops A and B are of different electrical length or otherwise have different electrical parameters that can effect signal latency. Because the received symbols are concurrent by construction, the associated data bits may be recombined to reconstruct the original data stream without buffering.

20   As described above, the device and method of this invention preferably uses a form of "table directed" training whereby a known data sequence is

transmitted and then regenerated in the receiver. In the embodiments of Figs. 1-5, the training data comprises a sequence of 1's so that the output sequence can be easily regenerated. As is known to those of skill in the art, the scramblers 204A, 204B function as pseudo-random number generators to

5   randomize the input sequence. This prevents training and decision problems that can arise when the input data is constant. In the embodiment of the device and method described herein, the equivalent of a "table" is generated by training scrambler 304 and mapper 306 (Fig. 3). Those of skill in the art will recognize that other table directed or data directed training techniques

10   can be used.

The data combiner 230 works in a manner opposite of the data splitter 202 used in the transmitter 102. If the A channel bits are numbered 0,2,4, ... 16, and the B channel B bits are numbered 1,3,5,...17, then the two channels are combined by putting the bits in numerical order.

15   The described method is effective in systems where the maximum differential delay between loops A and B (106, 108) is sufficiently small that the delay can be accounted for in LEQ's 318A, 318B. In one embodiment of the system, the maximum differential delay is estimated to be less than one symbol. The differential delay is automatically factored in by B channel LEQ

20   318B in the placement of the "center tap" (equalizer coefficent) that grows during the Training mode. As delay difference increases, the center tap will

grow too close to the edge of the equalizer, thereby impairing performance. If the differential delay exceeds the maximum tolerable limit (e.g., several sysmbols) the LEQ 318B will simply not acquire a solution. The maximum difference in latency that can be tolerated in a particular embodiment is

5   dependent on the number of coefficients in the linear equalizer. The disclosed embodiment can tolerate several symbols worth of differential latency, or around 1 msec.

Figs. 4 and 5 show alternate embodiments of the dual transceivers 102, 104. In these alternative embodiments, a second descrambler 410 and

10   demapper stage 510 are added for generating Training mode data for Loop B. This enhancement addresses a problem that could occur in the simpler implementations shown and described with reference to Figs. 2 and 3. In the first embodiment (Figs. 2 and 3), both loops A and B (106, 108) are trained using identical symbol streams in the training data. This renders the

15   receivers 220A, 220B incapable of estimating and reducing the effects of crosstalk between the wire pairs. The embodiment of Figs. 4 and 5 resolves this problem by descrambling the transmit symbols using a polynomial that is unrelated to the scrambler polynomial. In so doing, the data for channel B/Loop B is randomized with respect to channel A/Loop A in a predictable

20   way, such that the table directed training can still occur in the receiver.

Fig. 6 illustrates the modes of operation of the dual transceivers 102, 104 of the present invention. At start-up, the device enters a Pre-training mode. There is an exchange of tones, followed by an FSK-modulated exchange of pre-training data. The pre-training data is used to assign

5   channel A and channel B, to determine whether there are load coils present or not, and to estimate the line losses for setting the automatic gain control. The Pre-training mode and Training mode are active during startup. The Data mode is functional during data transfers between the C-end and the R-end. The transceivers 102, 104 may be used in an "always on" environment

10   and remain on for extended periods of time unless interrupted for maintenance, power failure or some other reason.

Fig. 7 contains a flow diagram of a typical equalizer training sequence used in the Training mode, in accordance with the present invention. During equalizer training, the transmitter corresponding to the opposite end from

15   the receiver sends the same sequence of symbols (scrambled 1's) on each A and B channel. In the second embodiment of Figs. 4 and 5, the scrambled 1's for the channel B transmitter are passed through the second descrambler 410, producing an uncorrelated (but derivable) symbol sequence. Thus, in the embodiment of Figs. 4 and 5, the A and B channels are using different

20   sequences in the Training data. However, the channel B sequence is derived from the channel A sequence, so that training can still occur.

As mentioned above, in a preferred embodiment of the system, table directed training is used. At the beginning of the Training mode, the channel A receiver trains with the channel B receiver, for all practical purposes, turned off. The channel A receiver is provided with a simple compromise equalizer LEQ 318A that allows it to begin to make decisions about the transmitted symbols. Thus, at the beginning of the Training mode, channel A is trained with a decision directed train. The system knows what sequence of training symbols is being transmitted because the polynomials used in the scrambler 204A are known. Once the equalizer makes enough correct decisions (determined by the bit length of the descrambler), the information from the descrambler is forced into the scrambler. The LEQ and DFE coefficients for channels A and B are reset by, for example, being zeroed out. Both channels A and B are now training using the acquired set of symbols, with the scrambler outputs as the decisions. In the embodiment of Figs. 4 and 5, the second descrambler 410 outputs are used. In this novel method, table directed training is used to force synchronization between the A and B channels. By forcing the same training data through each channel together in this manner, signals that are time aligned in the transmitter in the Data mode will always be time aligned in the receiver. Consequently, the transmitted data stream can be reconstructed in the receiver without any additional buffering.

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Thus, in accordance with one novel feature of the invention, receiver parameters, such as equalizer coefficients, are adjusted during the Training mode to functionally eliminate any differential delay between loop A and loop B. These adjustments are made by sending identical training data down the

5   A and B channels and forcing the two channels to train together. The operational result of these adjustments is that any delay introduced into the system by one loop is also created in the other loop so that data signals that are time aligned in the transmitter are also time aligned in the receiver.

During the Training mode, uncoded 4-QAM modulation is used. In a

10   preferred embodiment, more than one constellation will be used. The coded 1024-QAM constellation is the largest used for the Data mode.

At the highest data rate, the payload of the system is 64 kbps and the overhead in 800 bps. Transmission reach is less than 50 kft, or with insertion loss less than 10 dB at 1004 Hz. Several symbols of differential

15   delay can be accounted for (e.g., 500 usec to 1 msec), depending on the length of the linear equalizer.

Those of skill in the art will recognize that additional functional components, conventional in nature, may be added to a transceiver implementation of the present invention to provide improved performance,

20   such as a Tomlinson pre-coder, and a trellis encoder/decoder. One embodiment of a transceiver that includes such functional components is

illustrated in Fig. 8, wherein the upper portion of the diagram shows the transmitter and the lower portion shows the receiver. The transceiver of Fig. 8 can be located at either the remote end or the central office end of the loop. In the central office end, the timing is locked to the 8 kHz reference clock. In

5   the remote end, the timing is locked to the received signal, hence indirectly locked to the central office 8 kHz reference clock.

The data input to the transmitter begins with a scrambler, followed by a serial to parallel converter which converts from a serial bit stream into the number of parallel bits required by the trellis encoder. The trellis encoder

10   receives K parallel bits every symbol time and outputs a complex discrete value or voltage. The trellis encoder output passes through a Tomlinson precoder, also producing a complex discrete value (voltage). The Tomlinson precoder is a non-linear filter that simultaneously pre-equalizes the channel and whitens the output. The Tomlinson precoder output passes through a

15   QAM modulator, providing a real discrete value. In addition, the Tomlinson precoder output passes through the echo canceller to produce the real echo replica. An interpolator receives the output of the modulator and changes the time base from the central office timing to the local 18 kHz timing. The output from the interpolator is then sent through a digital-to-analog

20   converter to the analog hybrid.

The receiver input begins with an A/D converter that produces a real, discrete value, followed by an interpolator to change the time base from the local 18 kHz timing to the central office timing. The interpolator output is supplied to a decimator, which reduces the sample rate to three times the

5 symbol rate, and then the real discrete echo replica is subtracted. After subtracting the echo replica, the signal passes through a QAM demodulator, producing a complex discrete value, followed by a linear equalizer and a modulo device. The resulting complex discrete value is decimated by 3 (reducing the sample rate to the symbol rate) and passed into the trellis

10 decoder. The output of the trellis decoder is K parallel bits that are converted to a serial stream and passed out of the receiver through the descrambler.

The timing loop and the echo canceller are functionally positioned between the transmitter and the receiver. The echo canceller models the echo channel between the output of the Tomlinson precoder and the input to

15 the echo replica subtractor. The timing loop drives the hardware timing generator to produce a signal which is phase and frequency locked to the central office end, which in turn is used to produce the bit and symbol clocks, and to determine the correct interpolator setting.

It will be apparent to those of skill in the art that the method of this

20 invention can be extended to three or more wire pairs. The method can also be used with loops that have load coils attached.

Thus, although there have been described particular embodiments of the present invention of a new and useful Method and Apparatus for Duplex Transmission on a Four Wire Communication System, it is not intended that such references be construed as limitations upon the scope of this invention

5   except as set forth in the following claims.